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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,346	03/29/2004	Yoshiharu Ogata	81754.0120	2693

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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,346	OGATA, YOSHIHARU	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *3, 8-10 and 12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03-29-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of Embodiment II of Group I, claims 1, 2, 4-7 and 11 in Paper No. 2 is acknowledged.

Drawings

2. Figure 11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 2, 4, 6 and 11 are rejected under 35 U.S.C. 102(a) as being anticipated by Chen et al. (US Pat. Application Pub. 2002/0096754).

Regarding claims 1, 2 and 4, Chen et al. disclose a semiconductor device (Fig. 2) comprising:

- a substrate provided with terminals (22 and 26 respectively in Fig. 2) for connecting conductive wires
- a first semiconductor chip/integrated circuit (IC) mounted face-up on the substrate and electrically connected to the terminals provided on the substrate by the conductive wires (see 34 and 44 respectively in Fig. 2), and
- a second semiconductor chip/IC having recesses and a projecting part (see 46/51 in Fig. 2) formed on a rear surface thereof and attached onto the first semiconductor chip via the projecting part, and
- an adhesive/insulating resin that attaches the second semiconductor chip/IC onto the first semiconductor chip/IC via the projecting part and fills regions of the recessed/stepped part of the projecting part (see 52 in Fig. 2)

(Fig. 2, sections 0020-0025).

Regarding claim 6, Chen et al. teach the entire claimed structure as applied to claim 1 above, wherein Chen et al. further teach:

- first bonding/electrode pads (42 in Fig. 2) provided on the first semiconductor chip/IC
- first conductive wires (44 in Fig. 2) electrically connecting the first electrode pads to the terminals provided on the substrate

- second bonding/electrode pads (42 in Fig. 2) provided on the second semiconductor chip/IC
- second conductive wires (44 in Fig. 2) electrically connecting the second bonding/electrode pads and the terminals provided on the substrate
- the adhesive/insulating resin (50 in Fig. 2) provided between the first semiconductor chip/IC and the second semiconductor chip/IC so as to be present below the second bonding/electrode pads and attaching the second semiconductor chip/IC onto the first semiconductor chip/IC via the projecting part.

Regarding claim 11, Chen et al. teach the entire claimed structure as applied to claim 1 above, wherein Chen et al. teach the device comprising the first and the second semiconductor chips/IC/electronic components (Fig. 2, sections 0020-0025).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. Application Pub. 2002/0096754) in view of LoBianco et al. (US Pat. 6340846).

Regarding claim 5, Chen et al. teach the entire claimed structure as applied to claim 1 above, wherein Chen et al. further teach:

- first bonding/electrode pads (42 in Fig. 2) provided on the first semiconductor chip/IC
- first conductive wires (44 in Fig. 2) electrically connecting the first electrode pads to the terminals provided on the substrate
- second bonding/electrode pads (42 in Fig. 2) provided on the second semiconductor chip/IC
- second conductive wires (44 in Fig. 2) electrically connecting the second bonding/electrode pads and the terminals provided on the substrate
- the adhesive/insulating resin (50 in Fig. 2) enclosing a portion of the first conductive wires on the first semiconductor chip/IC and attaching the second semiconductor chip/IC onto the first semiconductor chip/IC via the projecting part.

Chen fails to teach a sealing resin sealing the first semiconductor chip to which the first

conductive wires are connected and the second semiconductor chip to which the second conductive wires are connected.

LoBianco et al. teach a stacked device (see Fig. 6) wherein an insulating adhesive/encapsulate resin (see 64/60 in Fig. 6) is formed to seal the first and the second semiconductor chips/IC and respective wires (see 14, 16, 38 and 64/60 in Fig. 6; Col. 5).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the sealing resin sealing the first semiconductor chip to which the first conductive wires are connected and the second semiconductor chip to which the second conductive wires are connected as taught by LoBianco et al. so that the desired protection for the chips and the bonding wires can be achieved in Chen's device.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. Application Pub. 2002/0096754) in view of Eguchi et al. (US Pat. 6784541).

Regarding claim 7, Chen et al. teach the entire claimed structure as applied to claim 1 above, except an insulating layer formed on an entire rear surface of the second semiconductor chip including the projecting part.

Eguchi et al. teach a device (see Fig. 7C-7H) wherein an insulating resin/layer (see 7 in Fig. 7C) is formed on an entire surface/rear surface opposing the surface having connection pads to provide the desired thermal dissipation (Col. 11 lines 1-16).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating layer formed on an entire rear surface of the second semiconductor chip including the projecting part as taught by Eguchi et al. so that the surface protection and thermal dissipation can be improved in Chen's device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

05-05-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800